AMENDMENTS TO SPECIFICATION:

Please replace the paragraph beginning at page 2, line 4, which starts with " Thus, a need exists for a method of implementing **", with the following amended paragraph:**

Thus, a need exists for a method of implementing analog circuits within a low voltage digital CMOS process with reduced jitter and expanded voltage ~~head room~~ headroom.

Please replace the paragraph beginning at page 2, line 9 , which starts with " One object of the present invention is to provide **", with the following amended paragraph:**

One object of the present invention is to provide an voltage controlled oscillator, VCO, suitable for integration in a low voltage digital CMOS process, in which the VCO's voltage ~~head room~~ headroom is not much reduced from its rail-to-rail voltage range.

Please replace the paragraph beginning at page 11, line 13, which starts with " As shown, the frequency output 103 of VCO 87 **", with the following amended paragraph:**

As shown, the frequency output 103 of VCO 87 closes the digital frequency difference loop and its phase output 105 closes the analog phase detector loop. This simple model may be used on a circuit simulator to investigate the effects of component bandwidths including the VCO modulation bandwidth, filter characteristics, pump currents, etc. Simulations on a Cadence SPECTRE® circuit simulator were used to select the values of components in an experimental test chip. Applying a frequency step input to this model showed that each frequency correction measurement is a time delayed frequency step which causes the analog loop to respond. Improper choice of measurement intervals, filters, and pump current can cause the two corrections to oscillate in opposite directions. However, when the measurement interval for

the digital frequency detector, i.e. the frequency sampling interval, is large compared to the bandwidth of the analog phase detection loop, the output Vf of the frequency detector can be regarded as a fixed value while the analog loop responds. The frequency transfer function then becomes the sum of two terms $[sKvVf/(s+K\phi R(s))] + [KvR(s)Fi/(s+KfR(s))]$, a fixed value contributed by the FDD and a variable term for the analog correction. This implies that the gain $K\phi R$ must be kept low in order for the frequency detector loop to dominate.

Please replace the paragraph beginning at page 13, line 18, which starts with " In the constructed test chip **", with the following amended paragraph:**

In the constructed test chip, the oscillator inductor was measured at 3.1 nH. Table I shows some of the characteristics of the experimental chip. The chip was operated at one voltage with a separate input pin for the VCO Vdd. The power was measured while the synthesizer was locked at 1.1GHz. Note that the summing amplifier passband was only 3MHz and so represented an upper limit on the open loop response of the analog phase detector loop. The size of the frequency counters determined a measurement interval of 131 μsec, corresponding to a high frequency response of ~~7.6KHz~~ 7.6 kHz for a minimum frequency step.

Please replace the paragraph beginning at page 14, line 5, which starts with " Measurements were taken to determine the effect **", with the following amended paragraph:**

Measurements were taken to determine the effect of operation of both loops simultaneously on lock range and jitter. Lock range for operation with the frequency loop alone was defined to be the region of stable loop operation. This is when the frequency difference detector indicated lock and only a difference corresponding to 1 LSB in the frequency counter was observed. This definition was used since there was no phase coherence with the input. When

both loops were operating simultaneously, the region of lock was defined as the frequency range for coherence with the input. Jitter was measured with an Agilent® 86100A, a ~~D~~digital ~~C~~communications ~~A~~analyzer, which combines deterministic and random jitter into one measured number.